

REMARKS

The Office Action mailed November 20, 2002, has been received and reviewed. Claims 19, 21 through 23, and 25 through 34 are currently pending in the application. Claims 19, 21 through 23, and 25 through 34 stand rejected. Applicant has amended claim 19, and respectfully requests reconsideration of the application in light of the amendments and remarks presented herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in View of U.S. Patent No. 6,002,177 to Gaynes et al.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Gaynes et al. (U.S. Patent No. 6,002,177). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicant submits that the obviousness rejection of claim 19 is improper because the prior art references fail to teach or suggest all of the limitations of the presently claimed invention and because there is a lack of motivation to combine the references as suggested by the Examiner.

Claim 19, as amended herein, is directed to a method of fabricating a multi-die assembly. The method comprises: providing a substrate including a plurality of conductors; attaching at least one active face-down base die to said substrate in electrical communication with at least some of said plurality of conductors; *providing a layer of conductive epoxy adhesive to a back side of the at least one base die; placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive; curing the layer of conductive epoxy adhesive and securing the back side of at least one stack die to said at least one base die*; electrically connecting said at least one stack die directly to at least one of said conductors; *and electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack die.*

Yamauchi discloses a method of fabricating a multi-die assembly with at least two TAB chips “joined with an adhesive 7 with end faces having no bump 3 faced (sic) each other.” (Constitution). The bumps of the lower TAB chip are joined with solder to a printed board, and the bumps of the upper TAB chip are connected with wire leads which are joined to a pad of the printed board. Applicant notes that Yamauchi fails to teach or suggest that the adhesive used to join the two TAB chips includes a layer of electrically conductive epoxy. Furthermore, while the Examiner cites Yamauchi as teaching *electrically grounding at least one base die via the adhesive and at least one stack die*, the Examiner does not point to, nor does Applicant find, any specific teaching in Yamauchi regarding such subject matter.

Gaynes teaches a chip stack including a plurality of chip-to-chip interconnects configured to reduce the length of conductor paths among the chips. The individual interconnects may be formed by filling laser-drilled holes, formed in the individual chips, with an electrically conductive paste having transient liquid phase (TLP) properties. (See, e.g., col. 4, lines 21-42). An example of such paste includes tin coated copper particles mixed with a dielectric thermoplastic adhesive. (See, e.g., col. 7 lines 60-63). According to Gaynes, “[s]o-called transient liquid phase (TLP) metallurgical processes...are characterized by partial liquefaction of conductive metals occurring, with heating, *at an interface between alloying metals* which, beginning with a eutectic alloy, mix and solidify as the composition of the alloy changes,

simultaneously raising the melting point of the alloy as the materials mix and the alloy composition is altered.” (Col. 9, lines 30-39, emphasis added). Applicant submits that formation of the discrete chip-to-chip interconnects using a TLP conductive paste, as set forth in Gaynes, is a substantially different process than providing a layer of electrically conductive epoxy adhesive between two die and subsequently curing the epoxy adhesive such as is set forth in claim 19 of the presently claimed invention.

Applicant further submits that, since Gaynes fails to teach or suggest providing a layer of conductive epoxy adhesive between two in the manner set forth in claim 19, Gaynes also fails to teach electrically grounding the base die via such an electrically conductive epoxy layer.

Moreover, Applicant submits that Gaynes teaches away from Yamauchi as it teaches a plurality of discrete chip-to-chip interconnects disposed between two facing surfaces of adjacent chips. In contrast, Yamauchi expressly teaches that the chips are joined with an adhesive “with end faces having no bump 3 faced (sic) each other.” (Yamauchi, Constitution; see also FIG. 1). Applicant, therefore, submits that even if all of the limitations of claim 19 were taught or suggested by Yamauchi and Gaynes (which Applicant maintains to the contrary), one of ordinary skill in the art would lack motivation to combine the references such as suggested by the Examiner.

Applicant submits that claim 19, as amended herein, is clearly patentable over the Yamauchi and Gaynes, either considered alone or in combination, and respectfully requests reconsideration and allowance thereof.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in View of U.S. Patent No. 6,002,177 to Gaynes et al. and Further in View of U.S. Patent No. 5,323,060 to Fogal et al.

Claims 21 through 23, 25 through 29, and 33 through 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Gaynes et al. (U.S. Patent No. 6,002,177) and further in view of Fogal et al. (U.S. Patent No. 5,323,060). Applicant respectfully traverses this rejection, as hereinafter set forth.

The 35 U.S.C. § 103(a) obviousness rejections of claims 21-23, 25-29 and 33-34 are improper because the references relied upon by the Examiner fail to teach or suggest all of the limitations set forth in the presently claimed invention.

Claims 21-23, 25-29, 33 and 34 each depend from independent claim 19 either directly or through intervening claims. As set forth above, Yamauchi and Gaynes clearly fail to teach or suggest all of the subject matter of the presently claimed invention as set forth in independent claim 19. Particularly, Yamauchi and Gaynes fail to teach or suggest providing a layer of conductive epoxy adhesive, or grounding the base stack die through such a layer of electrically conductive epoxy adhesive. Additionally, as set forth above, there is a lack of motivation to combine Yamauchi and Gaynes as suggested by the Examiner.

Applicant further submits that Fogal fails to teach or suggest providing a layer of conductive epoxy adhesive or grounding the base stack die through such a layer of electrically conductive epoxy adhesive. Moreover, Applicant submits that Fogal teaches away from the presently claimed invention inasmuch as Fogal teaches that the “[a]dhesive 38 preferably comprises an electrically *insulating* layer.” (Col. 3, lines 8-9, emphasis added).

Additionally, Applicant submits that there is a lack of motivation to combine the teachings of the references relied upon by the Examiner as Yamauchi teaches back-to-back arrangements of the semiconductor dies while Fogal teaches face-to-back arrangements of semiconductor die with no apparent suggestion in either of such references that the teachings of one are applicable to the other.

Applicant, therefore, submits that claims 21-23, 25-29, 33 and 34 are allowable over Yamauchi, Gaynes, and Fogal, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in View of U.S. Patent No. 6,002,177 to Gaynes et al. and U.S. Patent No. 5,323,060 to Fogal et al. and Further in View of U.S. Patent No. 5,399,898 to Rostoker

Claims 30 through 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Gaynes et al. (U.S. Patent No. 6,002,177) and Fogal et al. (U.S. Patent No. 5,323,060), and further in view of Rostoker (U.S. Patent No. 5,399,898). Applicant respectfully traverses this rejection, as hereinafter set forth.

Each of claims 30-32 depend from claim 19 either directly or through intervening claims. As set forth above, Yamauchi, Gaynes and Fogal clearly fail to teach or suggest all of the subject matter of the presently claimed invention as set forth in independent claim 19. Particularly, Yamauchi, Gaynes and Fogal fail to teach or suggest providing a layer of electrically conductive adhesive and grounding the base stack die through the layer of conductive epoxy adhesive. Applicant further submits that Rostoker fails to teach or suggest such subject matter.

Additionally, Applicant submits that there is a lack of motivation to combine the teachings of the references relied upon by the Examiner as Yamauchi teaches back-to-back arrangements of the semiconductor dies while Rostoker teaches face-to-face arrangements of semiconductor die with no apparent suggestion in either of such references that the teachings of one are applicable to the other.

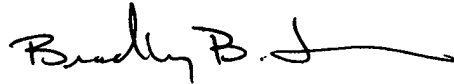
Moreover, with respect to claims 31 and 32, while the Examiner points to FIG. 4A of Rostoker as teaching the subject matter of bridging two base die with a stack die, Applicant submits that one of ordinary skill in the art would lack motivation to combine such a teaching with Yamauchi. Rostoker explicitly states that such an embodiment requires increased substrate surface area (see, e.g., col. 15, lines 9-11) thereby teaching away from Yamauchi which states that its disclosed arrangement is desirable because it substantially *reduces* mounting area.

Applicant, therefore, submits that claims 30-32 are allowable over Yamauchi, Gaynes, Fogal and Rostoker, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

CONCLUSION

Claims 19, 21 through 23, and 25 through 34 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: February 20, 2003

BBJ/ps:djp

Enclosure: Version With Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

19. (Three Times Amended) A method of fabricating a multi-die assembly, comprising:
providing a substrate including a plurality of conductors;
attaching at least one active face-down base die to said substrate in electrical communication with at least some of said plurality of conductors;
providing a layer of conductive epoxy adhesive to a back side of the at least one base die;
placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive;
curing the layer of conductive epoxy adhesive and securing the back side of at least one [active face-up] stack die to said at least one base die [with electrically conductive adhesive];
electrically connecting said at least one stack die directly to at least one of said conductors; and
electrically grounding said at least one base die via said layer of electrically conductive epoxy adhesive and said at least one stack die.